508.58 MHz Non-stop Synchronous Counter as a Final Version

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In order to realize a single bunch mode, we have developed new tools. One of them is a 508.58 MHz non-stop synchronous counter. Previous time, just three years ago, we designed a 508.58 MHz non-stop synchronous counter which consisted of 16 bits and was constructed with commercialized integrated circuits (MOTROLA MC10E016). And the feature of a counter is already reported [1] [2]. Basing on the successful result, we proceeded the final version of a counter. The remarkable change in the latest version is that universal counters are expanded up to 30 bits.

In case of a single bunch mode, beam injection from the linac to the synchrotron proceeds at the rate of 60 Hz and 8 buckets in the synchrotron are filled with beams. Beams in 8 buckets are transferred to the storage ring and inserted into one bucket of the storage ring. Total time from the linac to the storage ring is almost one second which corresponds to 1 Hz. The injection time through all processes in 1 second is perfectly defined on the base of 508.58 MHz clock. If one clock of 508.58 MHz, which corresponds to about 2 nsec., is missed, a single bunch mode is never realized. Thus we have required a precise and very long time digital delay device up to 1 sec.. A 508.58 MHz non-stop synchronous counter will be available as a precise digital delay . In fact, a precise digital delay is very useful for not only beam injection from the linac to the synchrotron, but also beam diagnostics. So we decided to improve the original design of a 508.58 MHz non-stop synchronous counter completely. The main improvements is to increase from 16 bits to 30 bits which correspond to more than 1 second as a digital delay time at 508.58 MHz clock. But it is not easy to be cascaded to increase the bit width of the counter to meet the needs. Because an 8-bit binary counter MC10E016 in cascade connection more than two IC's does not work at over 475 MHz. Thus we had to look for an another counter. A new counter is 6-bit counter MOTOROLA MC10E136 which allows for the cascading of multiple E136's for wider bit width counters that operate at nearly the same frequency as the stand alone counter. With a new counter, we designed completely a new 508.58 MHz non-stop synchronous counter and added many functions to the new version. The concept of a new counter is summarized as follows:

(1) A 508.58 MHz synchronous counter consists of 30 bits.
(2) External reset or start input is equipped.
(3) 1/N (N:positive integer) programmable divider is changed manually.
(4) It is possible to select only one cycle or continuous with a switch.
(5) Digital delay time (an arbitrary number M ($1 \leqq M \leqq N$) can be set from VME or manual.
(6) An output signal is created in the condition of M equal to counting number.
(7) Total propagation delay time must be controlled with a digital delay.
(8) Output signals are fast NIM level.

Above functions are realized on an actual circuit pattern and shown in Fig.1. And each number in Fig.1 stands for each function above mentioned.

References

[1] Y. Kawashima et al., RIKEN Accel. Prog. Rep., 27, 157 (1993).
[2] H. Suzuki et al., 9th Symp. on Accel. and Tech., 252 (1993).

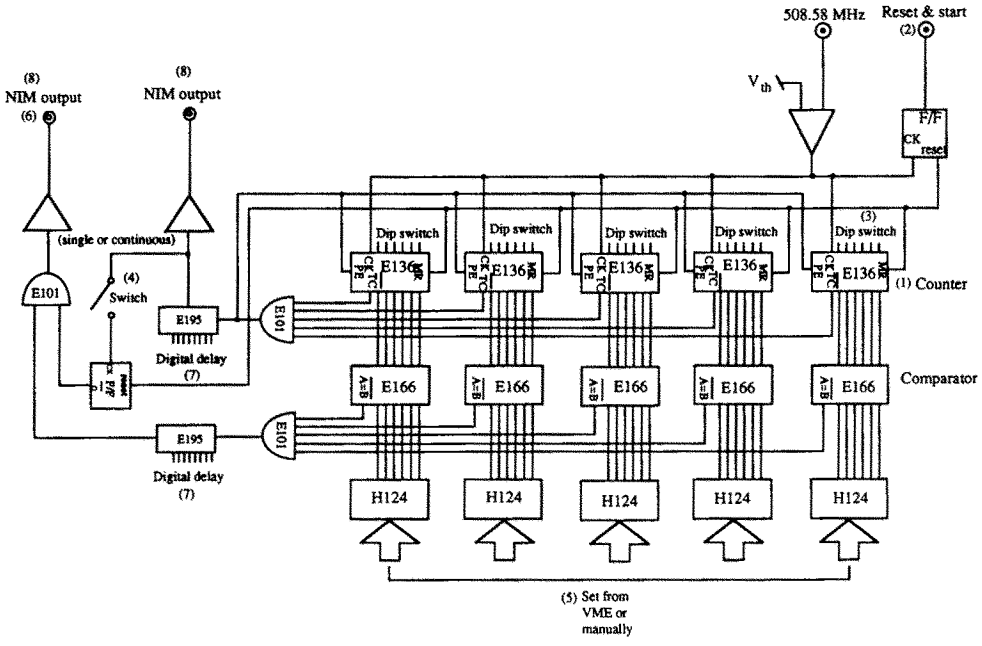

Fig.1. Layout of a 508.58 MHz non-stop synchronized counter. Used integrated circuits are all commercialized. Numbers in parentheses correspond to each functions. The circuit is packed in a 1-span NIM module.