Analog Processor for Emittance Monitor

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1. Introduction

Profile monitors are generally used for emittance measurement. For the SPring-8 linac, wire scanners are employed for emittance measurement [1]. When an electron beam impinges on the wire, secondary emission charge is generated. In order to detect the secondary emission charge, an analog processor was developed [2]. Because the efficiency is measured as 6~7% [3] for total surface at 0.03~1GeV, a high gain amplifier is required. The minimum charge is expected as ~0.01pC/pulse at the positron mode (1ns, 10mA). Therefore the maximum sensitivity of the analog processor is required as ~1V/pC to measure the positron beam profile.

2. Composition of Analog Processor

The analog processor is mounted on a print circuit board (see Fig. 1). The main components are a charge sensitive amplifier (CS-507, CLEARPULSE), a sample/hold IC (AD1154, ANALOG DEVICES), an adjusting circuit and an isolation circuit. Two diodes (PAD1, SILICONIX) are used for input protection. The PAD1 is a low leak diode which has specification of <1pA leak current. When the voltage exceeds ±6V at the input of CS-507, the extra charge is bypassed though the diode. The CS-507 is a hybrid IC which has a sensitivity of 1V/pC nominally, i.e. the built-in feedback capacitance is 1pF. The sensitivity can be changed by attaching external feedback capacitors. The sensitivities are designed as 1V/pC (high gain mode), 0.1V/pC (medium gain mode) and 1V/nC (low gain mode). Each time constant of relaxation is designed as ~1ms. The sensitivity can be changed by remote control. The CS-507 has the offset of ~-0.5V nominally. The AD1154 works to make a DC voltage from the pulsed signal of the CS-507. The adjusting circuit adjusts sensitivity and offset. The adjustable range is designed as 0.88~1.54. The isolation circuit breaks the ground inductor loop. If the impedance of the loop is low, a ground current flows. A ground current seriously degrades the S/N ratio.

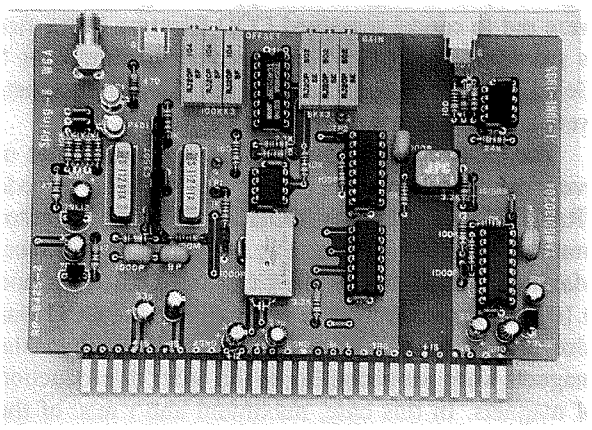

Fig. 1 Photograph of Analog Processor

3. Examination of Analog Processor

The analog processor was adjusted and examined using a simulated pulse. An appropriate reference capacitor Ci (10pF, 100pF or 0.01μF) was connected to the input of the analog processor. When a step voltage Vi was applied, a corresponding charge -CiVi was generated on the reference capacitor. The measured characteristics are summarized in Table 1. The linear region means the region where the output is proportional to the input within ±1%.

Table. 1 Measured sensitivity and linear region

Gain	High	Medium	Low
Linear Region	-6~+6 [pC]	-50~+60 [pC]	-5~+6 [nC]
Sensitivity	-1.0064 [V/pC]	-0.10030 [V/pC]	-1.0038 [V/nC]

References

[1] K.Yanagida, et al., Proc. of 1994 Linear Acc. Conf., Tsukuba, Japan, Aug. 1994, pp. 920-922.

[2] K.Yanagida, et al., Proc. of 10th Symp. on Acc. Sci. and Tech., Hitachinaka, Japan, Oct. 1995, pp. 144-146.

[3] R. Chehab, et al., IEEE Trans. Nucl. Sci., **NS-32**, 1953 (1985).