High Accurate Timing System for the SPring-8 Synchrotron

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Abstract

In the single-bunch-mode-operation, the accuracy with a low jitter and a high resolution is required for the timing system of the SPring-8 synchrotron. Previous to the timing system for the SPring-8, the test was carried out with a prototype of the timing system. It achieved specifications which have a jitter of 20 psec and a resolution of 20 psec. In this paper, the construction and some acquired data are reported.

1. Introduction

In the single-bunch-mode-operation, the injector (linac and synchrotron) injects 8 bunched beam into one bunch of the storage ring.

The synchrotron and the storage ring have 672 and 2436 buckets, respectively. A bunch in the synchrotron rounds 3 and 5/8 turns when a bunch in the storage ring rounds one turn. It means that for the effective injection, 8 bunched beam has to exist in interval of 84 buckets (1/8 of 672) in the synchrotron. Figure 1 shows the sequence of the single-bunch-injection.
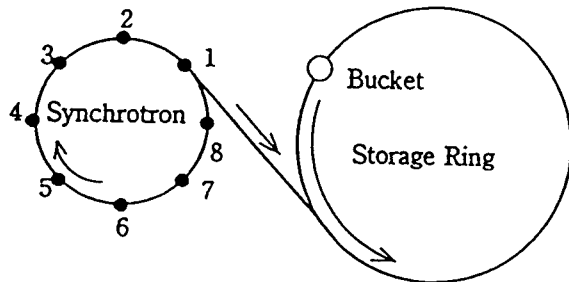
a) The bunched beam of #1 is injected to the storage ring.
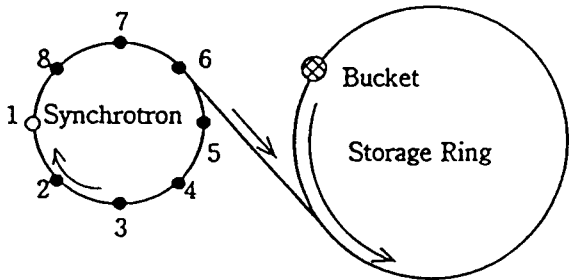
b) The bunched beam of #6 is injected when the bunch come to the injection point. Thus, eight bunches are injected to the same bucket of the storage ring. The order is #1,#6,#3,#8,#5,#2,#7 and #4.

Fig.1 The sequence of the single-bunch-injection

2. Requirement for the Timing System

For the single-bunch-mode-operation, following conditions are required.
(1) RF phase between the synchrotron and the storage ring is synchronized.
(2) Eight bunched beam in the synchrotron are located in the same interval correctly.

The first requirement is achieved, because the rf signal of the synchrotron is provided with low jitter by the timing system of the storage ring. The 2nd one is satisfied when the beam from the linac is injected into the designed bucket in the synchrotron. The pulse length of the beam from the linac is 1 nsec and the length of the bucket in the synchrotron is approximately 2 nsec.

The timing accuracy from the linac to the synchrotron has to be less than 100 psec.

3. Construction of the Test System

The prototype of the timing system is constructed and tested. The specifications are :

Input signal
    One-cycle signal   1Hz
    Master clock   508.58MHz
    Reset signal   1Hz
Output signal
    Linac trigger signal   8 pulses
    Start pulse   (for monitor)
    Clock   (for monitor)
Jitter   less than 100 psec
Resolution 100 psec
Function
    Generate 8 pulses for the linac trigger which has the interval of about 16.7 msec

The purpose of the system is to achieve an accurate linac trigger with a low jitter and a high resolution. Major components of the system are following four circuits.

3.1 Synchronized circuit

The synchronized circuit make synchronized clock signals from master clock(508.58MHz) and one-cycle signal.

3.2 Counter Circuit

a)Bunch-interval-counter

A bunch-interval-counter generates a bunch-interval-clock pulse in every 84 synchronized buckets. The cycle of this clock is equal to the interval time of the bunched beam of the synchrotron in the single-

interval-clock pulse in every 84 synchronized buckets. The cycle of this clock is equal to the interval time of the bunched beam of the synchrotron in the single-bunch-mode-operation.

b)One-turn-counter

A one-turn-counter generates eight signals which represent bunch numbers(#1-#8). These signals are rotated from #1 to #8 switched by the count of bunch-interval-clocks. These signals are used in the logic circuit to make a linac trigger pulse. This counter has its own delay-line for fine adjustment. The resolution of the delay-line is 20 psec.

c)Turn-number-counter

This counter counts the number of turns of an bunch in the synchrotron.

d)Injection-number-counter

3.3 Logic Circuit

A logic circuit generates eight linac trigger pulses. there are eight logic circuits(#1-#8) and each logic circuit represents the order of linac trigger. To select logic circuits, the one-turn-counter, the turn-number-counter and the injection-number-counter are used.

3.4 Output Circuit

An output-circuit makes linac-trigger-pulses with 10 nsec width and a delay-line. The range of the delay-line is selected from 0.1 nsec to 6.3 nsec by 0.1 nsec step. The resolution of this system depends on this delay-line.

The feature of this timing system are:

(1)A frequency-down-converter is not used, therefore it minimizes jitter and gets fine resolution.

(2) One high-speed-counter (ECL element) and some cascade-linked-counters are used. These counters select the logic circuit and control the timing of the linac-trigger-pulse. This system also minimizes jitter and high accuracy.

(3)A delay-line is used in the output circuit. This makes the adjustment of the delay timing easy.

4. Result

To confirm reliability, miscounts were checked and jitter through the timing system was measured.

4.1 Miscounts

With a universal time-interval counter, time interval between eight linac-trigger-pulses are measured. If there are N-times miscounts, the difference of time between maximum data and minimum data will be:

N x (cycle of clock)
= N x (1/508.58MHz)
= N x 1.966 nsec

The acquired data is shown in Table 1. Every time-interval is less than 1.966 nsec. It means there were not any miscounts.

Table 1 Data for miscount test

Signal	Δ(Tmax-Tmin)
#1-#2	0.45 nsec
#2-#3	0.49
#3-#4	0.55
#4-#5	0.45
#5-#6	0.55
#6-#7	0.53
#7-#8	0.45

4.2 Jitter

A digital sampling oscilloscope is used for the measurement. The acquired data are shown in Fig.2. The width of the sine-curve represents jitter of the linac-trigger-pulse. The jitter is about 20 psec after the fine adjustment of the delay line, this system satisfies the required specification for the single-bunch-mode-operation.
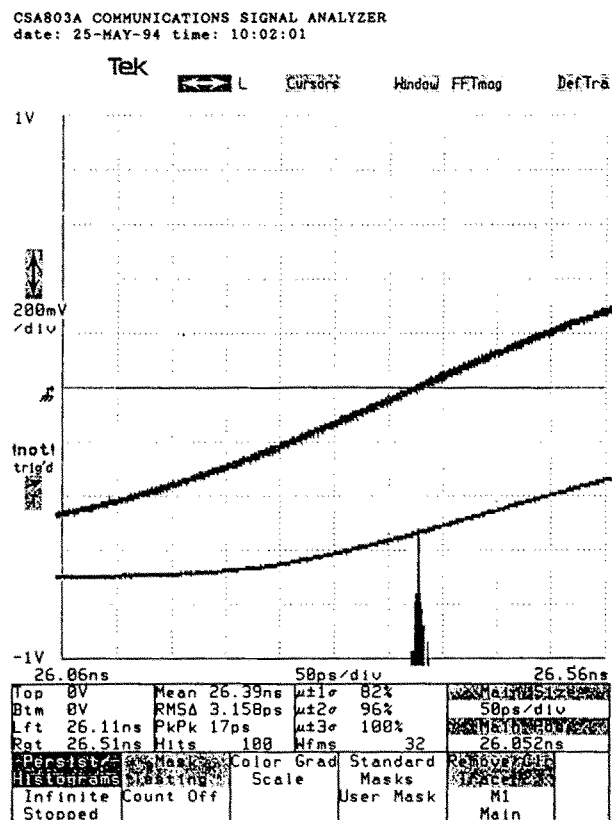

Fig.2 The jitter of the timing system

5. Conclusion

The required specifications for the timing system are achieved through the test system. The accuracy is around 20 psec, and the resolution is less than 20 psec. The timing system for SPring-8 synchrotron are under manufacturing. The element for the delay-line in the output circuit will be changed in this machine. This change will make the resolution higher up to 20 psec.