Control System

1. Status

In the last year, we finished the integration of the synchrotron control system to the SPring-8 standard system [1]. Since the new system started operation on January 1999, the system has proved to be stable and has recorded no downtime due to system failure as had sometimes occurred before.

The last accelerator control system to be integrated into the central controls is an injector linac system. We have already started R&D work finishing this up next year.

For the storage ring, an additional RF station was installed at the A-station area in the ring. An RF control system was constructed with the same architecture as that of other RF stations.

The year 2000 problem known as Y2K is one of the major problems to be solved before the first day of January, 2000. This summer we simulated accelerator operations as an exercise to confirm the Y2K readiness of the control systems.

1.1 Y2K readiness

The control system was one of the major facilities to be exposed to Y2K. The Y2K problem was seriously taken into account and control group was extensively collecting alert information concerning the reported problems. We surveyed around the computing system to list up known problems and replaced components or patched system defects during the summer shutdown.

In this work the HP-UX 9.0.5 operating systems were updated to 10.20, and the HP-UX 10.20 was also corrected with Y2K patches. The real-time operating system HP-RT 2.2.1 for VME was patched, and the network equipment firmware was updated to the latest version.

After these modifications, we performed a Y2K exercise with accelerator and beamline control software to follow a real sequence. We changed the date of the computing systems to simulate the crossover between 1999 and 2000. During the exercise two minor bugs were found such as an incorrect date display on a web browser and so on.

2. Electronics

2.1 New VME CPU Board

In the SPring-8 control system, we use HP9000/743rt CPU boards as VME device controllers. However, the supply of CPU boards was discontinued this November. It was necessary to find new CPU boards for the next generation. We decided to keep the VME-based CPU architecture in order to match the large amount of present VME-based I/O systems. Also it was essential to follow the open architecture philosophy to keep the selection range of sufficient width. We relied on readily available systems such as Intel-architecture CPUs and chip sets as the *de facto* standard.

The selection of the board operating system was left to free choice, that is, any OS which would run on Intel CPUs could be the successor at the beginning. The new operating system should satisfy real-time features and support the functions provided by the current operating system, HP-RT. Some promising candidates were Solaris and Linux, considering their open policy and future expandability. After studing the real-time features, we chose Solaris 7 as the first priority and Linux as a substitute OS.

Several candidate CPU boards were extensively investigated as well from the OS compatibility point of view. The board should be mounted with either a Celeron/Pentium or its compatible processor like AMD's. Also it would be necessarily to employ flash memory as a boot device and a bus-bridge interface chip between the PCI-bus and the VME-bus. The board will be determined after examination of various factors such as measurements of data transfer speed and interrupt latency from the VME-bus and so on.

2.2 Migration of Software Framework

We ported framework software running on the HP-RT to the Solaris system. The migration was easy because the software was written using UNIX systemV and POSIX system calls. Solaris has real-time class, however we manage the control processes in ordinary time-sharing class rather than real-time class. In time-sharing class, although the system scheduler controls the priority of processes, it is possible to maintain the order of priorities by changing the offset priorities. For example, the EM is usually running at a higher priority than that of the poller. Whenever the poller needs to lock a device shared by the EM, the priority of the poller can be dynamically set higher to avoid a deadlock.

2.3 VME I/O Boards

Stand-alone 16-channel pulse motor controllers (PM16C) were widely installed into the control systems of beamlines and experimental stations. The controller driven via GP-IB was useful in the early phase of beamline pre-commissioning because it was possible to control the pulse motors with no software. But the GP-IB communication rate was fairly slow and drove only two motors simultaneously. Consequently, because of the limitation of the control throughput, it was unsatisfactory for fast operation of the monochromators to adjust four axes to change the X-ray beam energy.

This year, new 8-channel pulse motor controllers (ADVME 2005) were introduced to the newly constructed beamlines. We kept the compatibility of the motor control messages. The communication overhead between the VME computer and the pulse motor controller was improved. As a consequence the control overhead from the user's computer was improved especially for the spectroscopy beamlines. Next year, we plan to modify the software framework by introducing a command interpreter (CI) software for monochromater operation to support any number of motors simultaneously.

3. Network

3.1 Backbone Upgrade

Before summer 1999, the accelerator control network consisted of FDDI backbones, and the beamline network was connected to the backbone via routers. At the beginning the routers were installed to separate the control network segments between the accelerators and beamlines.

In summer 1999, we additionally installed a high performance network system based on Gigabit Ethernet switching technology. The FDDI and Gigabit backbone was classified to play a role as follows; 1) the FDDI is used to control equipment with fault-tolerance in dual ring topology, 2) the Gigabit network is used as a data acquisition network with a high bandwidth.

At the end of 1999, we replaced the beamline routers with Layer 3 switching HUBs. The Layer 3 switching HUB provides more bandwidth and the same function of IP routing.

We measured the performance of the Gigabit Ethernet system through the firewall. The firewall bandwidth was measured to be 370Mbps for no packet inspection but was degraded to 170Mbps with the inspection and network address translation.

3.2 Beamline Users LAN

The BL-USER-LAN, a network system for users in the experimental hall, had been configured since September 1998. The BL-USER-LAN provided 100Mbps bandwidth for the backbone and 10Mbps for each beamline. At the same time, we connected the BL-USER-LAN to the Internet by introducing network firewalls. This allows users to transfer experimental data to their home laboratories on-line via the network.

Recently the number of computers on the BL-USER-LAN increased because of the rapid construction of the beamlines. There was a danger that amount of network traffic might limit the bandwidth for the users.

After January 2000, the backbone of BL-USER-LAN will be updated to support a 1Gbps bandwidth introducing Gigabit Ethernet. Beamline up-link connections to the backbone will be updated from 10Mbps to 100Mbps at the same time.

We also plan to introduce Virtual LAN (VLAN) technology following the BL-USER-LAN hardware update. VLAN can separate individual network segments on the logical flat layer over the physical cable configuration. Therefore, the independence of each beamline segment can be established and incorrect accesses or broadcast packets from other beamlines can be completely shut out.

4. Database

4.1 Growth of Database

The database manages not only the parameters of the storage ring, synchrotron and beamlines, but also stores logging data about the machines [2]. The number of raw signals and combined signals in the on-line database increases from 9500 to 13700 mainly due to the new beamlines. The total amount of logged data stored in the archive database has grown from 26GB to 66GB during 1999.

4.2 Server

The server, a 4-way Hewlett-Packard K250, had serious trouble twice in 1999. One was disk trouble and another was an OS crash. The database server mirrors disks to enhance the reliability. The problem happened with a disk that was not mirrored by the operational fault. We have never experienced an operating system crash since the patch was applied.

The management task of a huge volume of data requires the server to run at high load. To reduce the heavy load on the server, we modified the data access functions and application software. The main effort was to reduce the amount of communication and number of connections. Several improvements were observed, however the increasing volume of data reached the limit of processor. We are planning to replace the servers next year.

4.3 Development

Recent developments on PC-based UNIX, especially Linux opens the way to running an enterprise database management system on popular and inexpensive hardware. We tested a Sybase adaptive server enterprise 11.9.2 on a 4-way Intel Xeon processor machine, following the previous test on a single CPU machine. Even though the test system lacked several functions such as *raw disk* and its physical memory was limited (<893MB), the performance satisfied our demands.

Non numerical data such as images from the beam monitoring system provides much information about

the accelerator system. To store and retrieve image data will greatly help accelerator study and development. We tested the imaging database system in the frame of the current database system. In the next year it will be possible to store image data about the real operation.

5. Beamline Controls

5.1 New Interlock System

The beamline interlock system has been constructed and has been working well since 1995 [3]. However, it was difficult to build up additional interlocks because each system was not completely isolated.

To overcome the inconvenience, a new interlock system named "Beamline Interlock 98" [4] was designed in 1998. In the new design we added protection logic to isolate each system and updated the graphic panel design to ease operability for the users.

In this system, alarm items were classified into seven levels such that level 7 and 6 generate beam abort signal according to human protection or device protection. The levels from 5 to 1 are classified as device protection without beam abort.

The interlock system is connected to the beamline workstation (BL-WS) via RS-232C. The BL-WS reads the interlock status and writes to the SPring-8 database. The data is stored in the archive database and can be accessed from all beamlines as well as the central control room. The construction of the new interlock system was finished by the summer of 1999.

5.2 Application of CI

Whenever operators inject electron beams to the storage ring, it is necessary to move gaps of insertion devices to their nominal positions. The predefined positions are different from each other. Before we introduced CI software, the operators moved ID positions sequentially using each GUI with ID by ID. It was very complicated and too easy to make an error. After we introduced CI, the CI encapsulated the differences between IDs, and enabled the injection preparation to be performed in one action. Because the injection sequence has been simplified and paralleled, the injection waiting time has been reduced to 2/3.

5.3 Interlock Monitoring

The beam-abort interlock module (BIM) accepts abort signals from the beamline interlock systems and the GAPA interlock system [3]. The BIM system tells the first arrival of abort signals and sends them to the safety PLC network. The signals are stored in the database via a VME-PLC link. However, some abort signals are given by the safety PLC independently without reference to the database.

In order to establish the source of the beam abort source and reason quickly, it is essential to have all of the necessary information at the same time. This year we connected the VME systems to the PLC of the BIM system with a serial line. Now all abort signals were taken by the same software scheme and stored in the database.

5.4 Facility of Beamline Interlock Simulator

The beamline interlock system has become user-friendly. Safety education is still important for experimental users as they become accustomed to the interlock system. The simulator facility of the interlock system was designed for the realistic training of the users.

The facility simulates the same function of the real beamline interlock without real hardware. Users can control the simulated beamline devices, for example shutters and valves using the graphic panel. The simulated device covers the components of the beamline and experimental hutch as well. The system will be constructed next year and a training program will be provided.

References

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[4] T. Matsushita *et al.*, "The development of the beamline interlock system", in this volume.