

Three-dimensional Topography using an X-ray Microbeam and Novel Slit Technique

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X-ray section topography is a powerful tool for the nondestructive crystallographic analysis of semiconductor materials. In such analysis, however, recent requirements are beyond the capability of conventional section topography due to the development of microstructured semiconductor devices. Not only is submicron resolution required, but also the cross sections to be examined are often parallel or perpendicular to the device surface or along a dislocation line. Three-dimensional (3D) X-ray topography is intended for the quick measurement of topography for such various cross sections of devices with submicron resolution [1]. In this article we describe the application of this new method to the defect analysis of a SiC diode.

Experiments were conducted at the undulator beamline BL24XU. A monochromatic X-ray beam (E = 15 keV) was focused on a sample using a bent cylindrical mirror. The half widths (at 1/e of the maximum) of the focused beam were 1.16 μ m and 1.04 µm in the horizontal and vertical directions, respectively. We used a special slit with a V-shaped crevice (V-slit) for microbeam X-ray diffraction (Fig. 1). The V-slit is a metal contact made of stainless steel with polished slanted edges and an opening angle of 4°, that has a sharp-pointed exponential transmission curve [1]. The diffraction beam impinges on the V-slit, through which a thin beam passes to reach a scintillation counter (SC). We can thus observe a small region Q, where the incident beam crosses the extended line (broken arrow) of the beam passing



Fig. 1. Experimental setup. An X-ray microbeam penetrates a sample and a diffraction beam impinges on the V-slit, through which a thin beam passes to reach a scintillation counter (SC). Scanning the sample produces 3D topography. The V-slit is a metal contact made of stainless steel with polished slanted edges.

through the slit, and scanning the sample position provides 3D topography. Although the image obtained involves blurring caused by the tailed transmission curve of the slit, deconvolution can effectively restore the image [1].

The sample examined is a 200 \times 200 μm^2 p-n diode fabricated on an 8°-off-cut (0001) 4H-SiC wafer (Fig. 2(a)). As shown in Fig. 2(b), slice topographs (SiC 0 0 20 reflection) were obtained by performing a z (depth) scan and an x-y scan at each z position. Figure 3(a) shows a slice image (log scale), in which we observed three screw dislocations (SD1, SD2, and SD3). To examine the depth distribution of the SDs, x-z-section topographs along the SDs were reconstructed (Figs. 3(b), 3(c), and 3(d)). The broken lines indicate the interface between the epilayer and the substrate (epi/sub interface). Since the z scale is six times greater than the x scale, the slight slant of the sample is exaggerated. These figures clearly indicate that the SD lines penetrate the epi/sub interface.



Fig. 2. Cross-sectional view of the sample SiC diode (a) and its slice topographs (b). The diode was fabricated on an 8°-off-cut (0001) 4H-SiC wafer (a). The slice topographs were obtained by performing a z (depth) scan and a 2D scan at each z position (b).

Figure 4(a) shows a slice topograph (linear scale) of a similar diode with a SiC 0 0 16 reflection, where we observe an SD located on an upwardly winding grain boundary. We performed an *x-y-z* scan in a small region including this SD and obtained the *x-y* and *x-z* topographs shown in Figs. 4(b) and 4(c), respectively. For the *x-z* cross-sectional images, we performed a deconvolution [1] to restore the image. Note that the two boundaries as well as the wafer surface become clear in the restored image Fig. 4(d). These boundaries are in good agreement with the p/n junction and epi/sub interface (broken lines). The image restoration can improve the spatial resolution from about 2 μ m to 0.5 μ m or less.



Fig. 3. Analysis of screw dislocations in a SiC diode. The *x*-*y* slice topograph (**a**) and *x*-*z* section topographs (**b**)-(**d**) were obtained from a 3D scan over the device region. The topographs show three screw dislocations (SD1, SD2, and SD3) that penetrate the epi/sub interface (broken lines).

We thus clarified that the V-slit method can provide a submicron-depth-resolved diffraction image. Such analysis is valuable for SiC devices because it is important to examine whether a defect is generated during epilayer growth, or is replicated from the substrate. The new method also meets various requirements in semiconductor analysis. In particular, its nondestructive, cross-sectional imaging is useful in the crystallographic analysis of recently developed layer-structured devices.



Fig. 4. High-resolution defect analysis of a SiC diode. The slice topograph shows a screw dislocation (SD) (a). An *x*-*y*-*z* fine scan around the SD was performed to obtain the *x*-*y* and *x*-*z* topographs (b)(c). Deconvolution provides the restored image, in which the two boundaries of the dislocation as well as the wafer surface become clear (d). These boundaries are in good agreement with the p/n junction and epi/sub interface (broken lines).

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